A Technique for Predicting Large-Signal Performance of a GaAs MESFET

HARRY A. WILLING, MEMBER, IEEE, CHRISTEN RAUSCHER, MEMBER, IEEE, AND PIETRO DE SANTIS, MEMBER, IEEE

Abstract—A method is described for accurately predicting the nonlinear microwave performance of GaAs MESFET devices. The method utilizes time-domain analysis and is based upon the experimentally characterized bias dependence of device–circuit model elements. Precise predictions are made of fundamental and harmonic power levels up to 6 dB of gain compression.

I. INTRODUCTION

A N ACCURATE nonlinear device model is a valuable tool for establishing microwave performance limits of GaAs FET devices. Model predictions of gain compression and of harmonic and intermodulation distortion will assist in the design of large-signal components such as power amplifiers, oscillators, and harmonic generators. Linear models which describe the small-signal electrical performance of GaAs FET's have been reported in the literature. Analytical expressions for calculating the bias dependence of some of the linear model element values have also been developed. However, no accurate large-signal GaAs FET model has been previously reported.

The investigations outlined below focus on the derivation of a comprehensive nonlinear circuit-type device model. It evolves from the experimentally determined bias and frequency dependence of device scattering parameters. The model was used with a time-domain analysis program to simulate large-signal waveforms. The simulations were made with the device in a common-source configuration and mounted in a 50-Ω system. The output waveforms were transformed into the frequency domain by Fourier analysis. The excellent agreement obtained among the experimental and model-predicted gain compression, third-order intermodulation, and harmonic output power levels supports the model validity.

II. DEVICE CHARACTERIZATION

The nonlinear model to be presented here is based on extensive experimental characterization of an arbitrarily selected (Texas Instruments, Inc.) GaAs MESFET. This
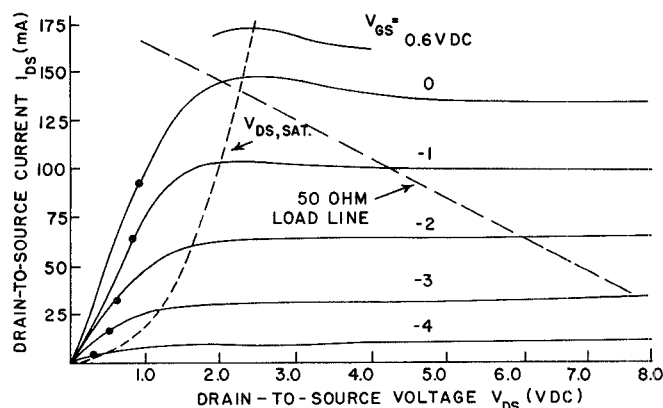
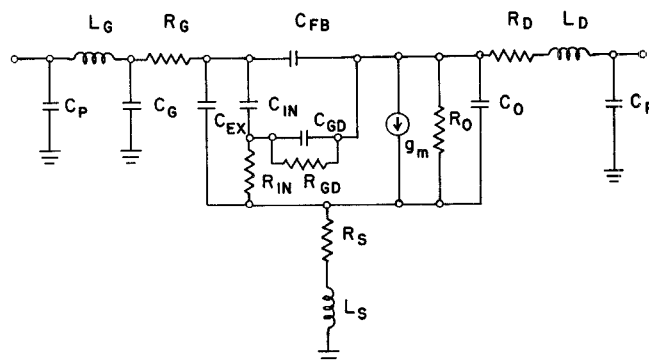Fig. 1. Measured static I_{DS}–V_{DS} characteristics.

Fig. 2. Circuit-type model of a GaAs MESFET. Package parasitic elements are L_S, L_G, L_D, and C_P. Fixed device elements are C_G, C_{EX}, C_{GD}, R_G, R_D, R_S, and C_0. Bias-dependent device elements are C_{FB}, C_{IN}, g_m, R_{IN}, R_{GD}, and R_0.

device has the following dimensional parameters:

gate width, l_w	600 μm
gate length, l_g	1.7 μm
epitaxial thickness, a	0.32 μm.

The measured device I_{DS} and V_{DS} curves are illustrated in Fig. 1. A nonlinear circuit-type model describing the large signal performance of this device was developed. The topology of this circuit-type model is identical to that of the linear model [1] previously described to include Gunn domain effects, as shown in Fig. 2. Development of the nonlinear model was based on the experimentally determined bias dependence of the small-signal device characteristics. S-parameter measurements were taken across
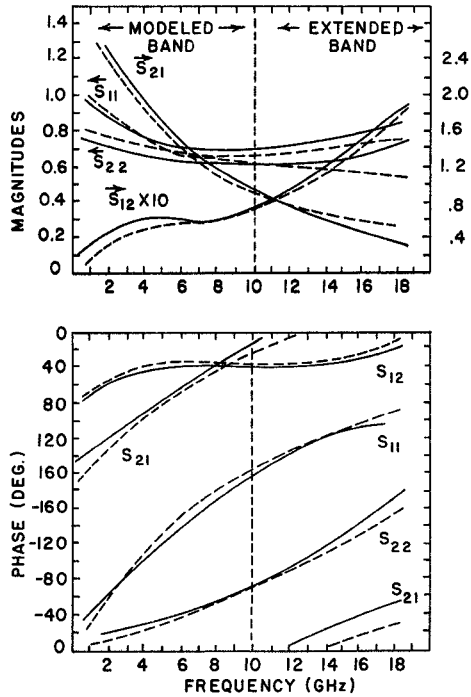
Fig. 3. S parameters (1–18 GHz) for a GaAs MESFET. Bias: V_{GS} = -2.0-V dc and V_{DS} = 6.0-V dc. Measured ———; Modeled - - - - -.

the frequency range of 1–10 GHz for discrete combinations of drain-to-source (V_{DS}) and gate-to-source (V_{GS}) voltages. The drain-to-source voltages covered the range of 0–8.0-V dc at gate-to-source voltage levels of 0.0, -1.0, -2.0, -3.0, and -4.0-V dc. The bias dependence of each element of the small-signal model was determined by the least square fitting of model-predicted S-parameters to the measured S-parameters for each bias condition. Initial sensitivity analysis indicated that the six model elements C_{IN}, R_{IN}, R_{GD}, C_{FB}, R_O, and g_m exhibited the strongest bias dependence and comprised the dominant device nonlinearities. Consequently, the other intrinsic model elements together with the package parasitics were considered to be linear elements and held fixed in value. Comparisons between model-predicted and measured S-parameters are displayed in Fig. 3 for the case of V_{DS} = 6.0 – V dc and V_{GS} = -2.0 – V dc. The good agreement in the 1–10-GHz band for which the model was established is shown to extend fully up to 18 GHz. The measurements in the extended frequency range were taken at a later date and were not included in the model optimization. The model predictions proved equally valid for the range of bias conditions required to develop the complete nonlinear model. The device characterization ultimately led to families of curves depicting the bias dependence of each of the six nonlinear model elements. These curves are shown in Figs. 4(a)–(f). Each curve reflects the response of the associated computer-fitted small-signal (incremental) model-element value to variations in the drain-to-source voltage with a fixed gate-to-source voltage. These curves form the basis for the development of the proposed nonlinear model.
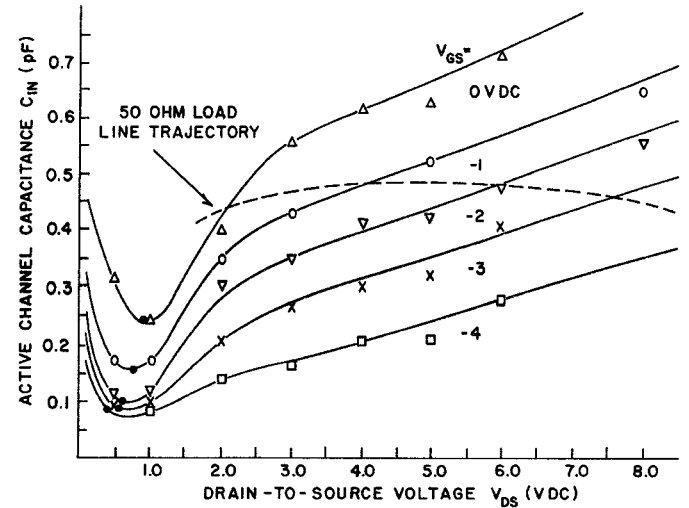
(a)
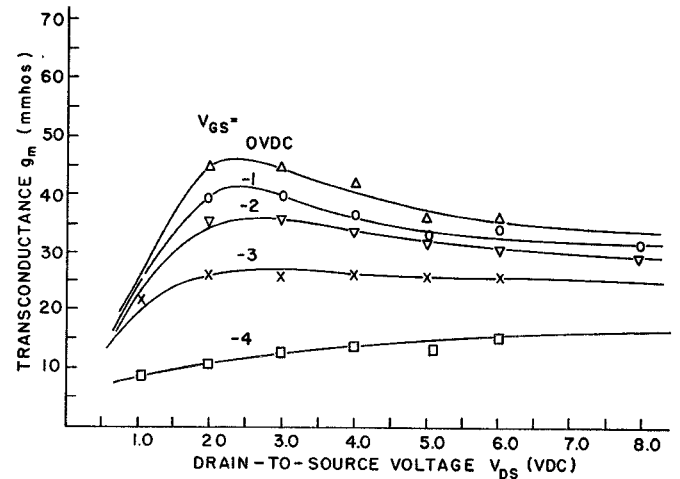
(b)
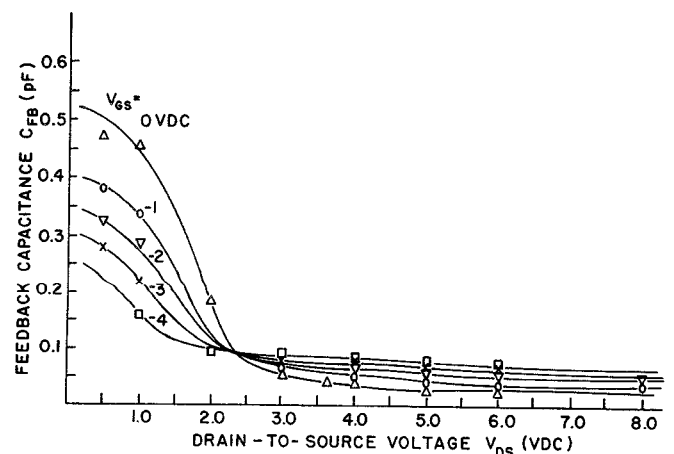
(c)

Fig. 4. Bias dependence of nonlinear model elements for a GaAs MESFET gate-to-source bias condition: $\triangle$ – V_{GS} = 0-V dc, $\bigcirc$ – V_{GS} = -1.0-V dc, ∇ – V_{GS} = -2.0-V dc, x – V_{GS} = -3.0-V dc, and $\square$ – V_{GS} = -4.0-V dc. (a) Active channel capacitance-C_{IN}. (b) Transconductance-g_m. (c) Feedback capacitance-C_{FB}.
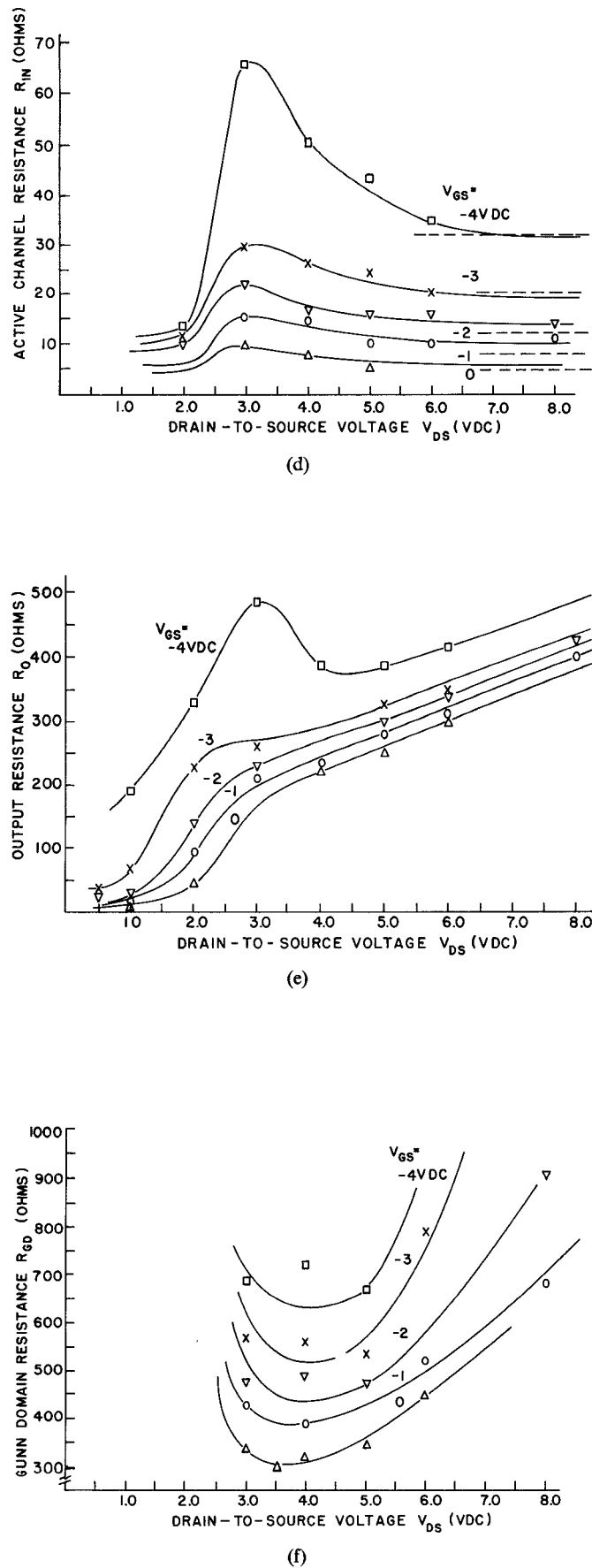
(d)

(e)

(f)

Fig. 4. (d) Active channel resistance-R_{IN}: --- $(1-{}^u m)^{-1}(G_{m0})^{-1}$. (e) Output resistance-$R_O$. (f) Gunn domain resistance-R_{GD}.

III. DISCUSSION OF BIAS INFLUENCE ON MODEL ELEMENTS

Studies were made to achieve a better understanding of the bias-dependent behavior of the small-signal (incremental) values of each nonlinear model element as shown in Fig. 2. The experimentally derived element values were compared to analytical values determined from the model of Lehovec and Zuleeg [2] at the onset of drift velocity saturation. The dimensional parameters of the device contained in the analytical model-element expressions of [2] are listed in the previous section. The required material and electrical parameters are as follows. DC measurements indicated the source-to-gate voltage (V_{GS}) required for the pinch-off to be approximately -5.1-V dc. The barrier or built-in potential (V_b) of the gate-to-channel junction is 0.7-V dc resulting in a channel pinch-off voltage (V_0) of -5.8-V dc. Using [2, (6)] and assuming a uniform doping profile, the doping density (N) was determined to be $7.5 \times 10^{16} \text{cm}^{-3}$. This value was found to be consistent with results obtained from CV-profiler measurements. Values for the low-field mobility (μ) of $4.24 \times 10^3 \text{cm}^2/\text{V} \cdot \text{S}$ and saturation drift velocity v_m of 1.83×10^7 cm/s were calculated from [2, (10) and (11)]. Values of the saturation current for the Shockley case (I_p) used in [2, (10)] and the velocity limited drain current (I_0) used in [2, (11)] were determined through extrapolations of the static V_{DS} and I_{DS} measurements. The analytical values for model elements C_{IN} and g_m were determined at the bias conditions required for the onset of drain-current saturation. The conditions are designated by the curve $V_{DS,SAT}$ in Fig. 1. The values of $V_{DS,SAT}$ were established from laboratory measurements and [2, (2)]. The dimensional and material parameters of the device together with the specified electrical parameters at the onset of current saturation satisfied the requirement of [2, (12)]. These parameters are used in the calculations referenced in the following discussions of some aspects of the bias-dependent behavior of each of the nonlinear elements.

A. Active Channel Capacitance (C_{IN})

The influence of bias on the active channel capacitance C_{IN} is illustrated in Fig. 4(a). The intially decreasing values of C_{IN} with increasing V_{DS} and constant V_{GS} are a result of an increasing depletion width. The active channel capacitance C_{IN} approaches a minimum at values of V_{DS} (indicated by symbol "·" in Figs. 1 and 4) where the drain-to-source current (I_{DS}) begins to saturate. This occurs in the region where the $I_{DS}-V_{DS}$ curves are no longer ohmic (maintain constant slopes). For further increases in V_{DS}, C_{IN} increases monotonically. This behavior was first reported by Engelmann and Liechti [3]. The phenomenon is attributed to charge accumulation effects in the channel. Projected plots of the total gate-to-source capacitance derived from the CV-profiler and S-parameter measurements displayed a fixed capacitance or total device excess capacitance of approximately 0.3 pF. This excess capaci-

TABLE I
BIAS DEPENDENCE OF DEVICE[1]-CIRCUIT PARAMETERS AT ONSET OF CURRENT SATURATION

V_{GS} (VDC)	$V_{DS,SAT}$ (VDC)	$g_{m(CALC)}$[2] ($\times 10^{-3}$ mho's)	$g_{m(FITTED)}$ ($\times 10^{-3}$ mho's)	$g_{m(DC)}$[3] ($\times 10^{-3}$ mho's)	$C_{GS(CALC)}$[2] (pF)	$C_{GS(FITTED)}$ (pF)
0.0	2.3	50	47	45	0.76	0.76
-1.0	2.0	37	40	41	0.65	0.63
-2.0	1.65	31	32	35	0.49	0.53
-3.0	1.2	25	22	25	0.35	0.40

[1] Texas Instruments, Inc., 600 $\mu m \times 1.7$ μm.

[2] Expressions of Lehovec and Zuleeg [2] at onset of saturation.

[3] Determined from I_{DS} and V_{DS} characteristics.

tance is simulated by elements C_G and C_{EX} of the model (see Fig. 1). Expression (26) of [2] was used to calculate the analytically modeled gate-to-source capacitance $C_{GS(CALC)}$ value. In Table I the calculated $C_{GS(CALC)}$ values are compared with $C_{GS(FITTED)}$ for the associated bias conditions. $C_{GS(FITTED)}$ is defined as being equal to the sum of the total excess model capacitance $(C_G + C_{EX})$ and C_{IN}, as shown in Fig. 2.

B. Transconductance (g_m)

The experimentally derived model element values of the transconductance $g_{m(FITTED)}$ are compared to both the values $g_{m(dc)}$ determined from the static $I_{DS}-V_{DS}$ characteristics and the value $g_{m(CALC)}$ calculated from the analytical expression [2, (17)]. The values were determined for the (V_{GS}, V_{DS}) bias conditions required for the onset of current saturation. Table I lists the values of $g_{m(CALC)}$, $g_{m(FITTED)}$, and $g_{m(dc)}$ at the indicated bias conditions. Good agreement exists between each set of values.

The complete set of bias-dependent curves illustrating the behavior of $g_{m(FITTED)}$ is depicted in Fig. 4(b). The decreasing values of g_m observed for values of V_{DS} greater than $V_{DS,SAT}$ were reported by [3]. This effect diminishes as the value of V_{GS} is increased and is attributed to a reduction in charge accumulation effects.

C. Feedback Capacitance (C_{FB})

The effects of the charge accumulation at the drain edge of the gate is evident in the response of the feedback capacitance (gate-to-drain) C_{FB}, as shown in Fig. 4(c) and in [3]. A sharp reduction in the value of C_{FB} occurs as V_{DS} approaches $V_{DS,SAT}$. This effect diminishes with increasing $|V_{GS}|$. Above $V_{DS,SAT}$, the feedback capacitance increases with increasing $|V_{GS}|$.

D. Active Channel Resistance (R_{IN}) and Output Resistance (R_O)

The bias-dependent characteristics of the active channel resistance (R_{IN}) and output resistance (R_O) are illustrated in Figs. 4(d) and (e).

In Fig. 4(d) it can be observed that under low drain-to-source voltages (V_{DS}) the value of R_{IN} with constant V_{GS}

increases with increasing V_{DS}. The rate of increase becomes sharper with larger fixed values of $|V_{GS}|$. At higher drain-to-source voltages, the value of R_{IN} decreases and asymptotically approaches a constant resistance value. An empirical relationship $(1 - u_m)^{-1} G_{m0}^{-1}$ was found to describe the dependence of this asymptotic behavior on V_{GS}. The parameters in this relationship were previously defined in [2]; G_{m0} is the open channel transconductance as defined by (15). The parameter $(1 - u_m)$ is the ratio of the channel width at the drain edge of the gate when biased at $V_{DS,SAT}$ to the undepleted channel height derived from [2, (1)].

Fig. 4(e) shows the bias-dependent response of R_O starting from a resistance value approximating the ohmic or dc resistance of the device for $V_{DS} \ll V_{DS,SAT}$ and increasing with increasing values of V_{DS} or $|V_{GS}|$.

E. Gunn Domain Resistance (R_{GD})

The bias-dependent response characteristics of the Gunn domain resistance $(- R_{GD})$ was first reported in [1]. The influence of this negative resistance model element on the device characteristics increases as the value of $|- R_{GD}|$ approaches the value of R_O. Dependent upon the value of $|- R_{GD}|$, the magnitude of the output reflection coefficient S_{22} may approach or become greater than one. Normally $|S_{22}|$ can be expected to increase monotonically with increasing V_{DS} starting from the bias conditions where the slopes of the $V_{DS}-I_{DS}$ curves (V_{GS} constant) approximate 50 Ω. The influence of the Gunn domain resistance results in a nonmonotonic variation in $|S_{22}|$. This effect is most pronounced in the region of V_{DS} approximating $V_{DS,SAT}$ and low $|V_{GS}|$, i.e., high drain current. Increasing the gate-to-source voltage $|V_{GS}|$ reduces the negative resistance effects of the Gunn domain region. These characteristics can be seen in Fig. 4(f). The relative values of $- R_{GD}$ and R_O can be noted by comparing Figs. 4(e) and (f).

IV. PREDICTIONS OF NONLINEAR DEVICE-CIRCUIT INTERACTIONS

Large-signal circuit-type models for simulating nonlinear device-circuit interactions require expressions giving the instantaneous current-voltage relationships for each of the nonlinear model elements. The derivation of these nonlinear expressions from the bias dependence of the incremental (small-signal) element values depicted in Figs. 4(a)-(f) is discussed in the following. The instantaneous current through each model element is expressed as the product of an instantaneous element value and an instantaneous voltage or its time derivative. Thus each instantaneous element value takes on the dimension of either a conductance, a transconductance, or a capacitance and is a function of instantaneous voltages. The voltage v_1 across the input capacitance C_{IN} and the voltage v_2 across the drain-to-source resistance R_O are the independent vari-

ables used for describing this dependence. The incremental element values were previously characterized with respect to external dc voltages V_{GS} and V_{DS}. They can be expressed in terms of values for the internal voltages v_1 and v_2 by accounting for voltage drops across the device parasitic elements as shown in Fig. 2. It is assumed that these expressions remain valid under dynamic conditions where v_1 and v_2 then become time-varying voltages. It can be shown that the instantaneous element values are related to the corresponding incremental values through quasi-linear partial differential equations in v_1 and v_2. To solve these equations, two-dimensional polynomial expressions in v_1 and v_2 are fitted to the incremental parameter functions given in Figs. 4(a)–(f). The coefficients of the expansions can be found using nonlinear regression techniques. After substituting these expressions into the partial differential equations, numerical optimization techniques can be employed to determine the instantaneous element functions. They, too, are obtained in the form of two-dimensional polynomial expansions in v_1 and v_2. These expansions are then used to describe the instantaneous current–voltage relationships for each of the nonlinear model elements in Fig. 2. The present approach may thus be regarded as a generalization of earlier work [4]. The model in this form is capable of predicting the instantaneous currents and voltages at the device terminals with arbitrary load conditions. It is directly compatible with existing time-domain analysis programs and can be used to simulate nonlinear behavior of GaAs FET's in circuits such as power amplifiers and oscillators. A detailed description of the general procedure outlined above shall not be given here.

Comparisons between nonlinear performance predictions and measurements for the case of a GaAs MESFET with purely resistive termination are presented to validate the nonlinear model. This case was chosen to facilitate meeting the requirement that the terminations at the harmonic frequencies during simulation and measurement be consistent. The example is, however, general enough to represent a conclusive test for the basic technique. The resistive loading condition defines an interdependence between the two voltage variables v_1 and v_2 (independent variables for arbitrary loading). An approximate relationship describing this interdependence is used in the analysis of the resistive loading case to simplify the expressions for the various nonlinear model-element value functions. Each nonlinear element can then be described by only one independent variable. This results in a reduction in the complexity of the overall analysis. The relationship describing the interdependence between v_1 and v_2 is derived from the conditions imposed on static values of the two variables by the resistive load line indicated in Fig. 1. As illustrated for the case of C_{IN}, the bias conditions defined by the load line in Fig. 1 are superimposed on the families of curves in Fig. 4(a) and represented by the broken line. The incremental values of C_{IN} along this line

can be defined in terms of a single voltage variable (v_1 or v_2).

For the single-variable approximation to be valid, the frequency has to be low enough for the parasitic reactance effects to be negligible (maintaining the condition of resistive loading of the intrinsic device). The approximation was found not to noticeably degrade the accuracy of the simulation described in the paper. It should be emphasized that the load-line approximation is used only in simplifying the expressions for the voltage dependence of the nonlinear elements. The approximation does not enter into the circuit equations in any other constraining way.

The nonlinear transconductance is chosen as a representative example for illustrating the derivation of the polynomial expressions used to describe the nonlinear model elements. The incremental (small-signal) transconductance g_m and the instantaneous (large-signal) transconductance g_M can be shown to be related through the partial differential equation

$$g_m(v_1) = g_M(v_1) + \frac{\partial g_M(V_1)}{\partial V_1} \cdot v_1.$$

The equation evolves from the more complex equation in the two variables v_1 and v_2 after substituting for v_2 the relationship $v_2 = v_2(v_1)$ given by the resistive loading condition. The function $g_m(v_1)$ is derived from the experimentally determined bias dependence of the small-signal transconductance plotted in Fig. 4(b). To solve the equation, $g_m(v_1)$ is approximated by a polynomial expression of the form

$$g_m(v_1) = \sum_{k=1}^{n} \gamma_k v_1^{k-1}.$$

The instantaneous transconductance is then readily obtained to be

$$g_M(v_1) = \sum_{k=1}^{n} \frac{\gamma_k}{k} v_1^{k-1}.$$

Similar derivations are applied to all the other nonlinear model elements. This leads to the complete nonlinear model for the special resistive loading case under consideration. It should be noted that for output power levels approaching the 1-dB compression point the RF voltages will exceed the voltage ranges within which the nonlinear model elements have been characterized, as shown in Figs. 4(a)–(f). Outside these ranges extrapolations are used in defining the nonlinear element values. In addition, a diode was added in shunt with C_{IN} to represent the behavior of the Schottky-barrier junction under forward conduction.

This nonlinear model was used in conjunction with a commercially available time-domain analysis program (SYSCAP) to simulate device–circuit interaction for a device in a 50-Ω system. The modeled 600-μm device was
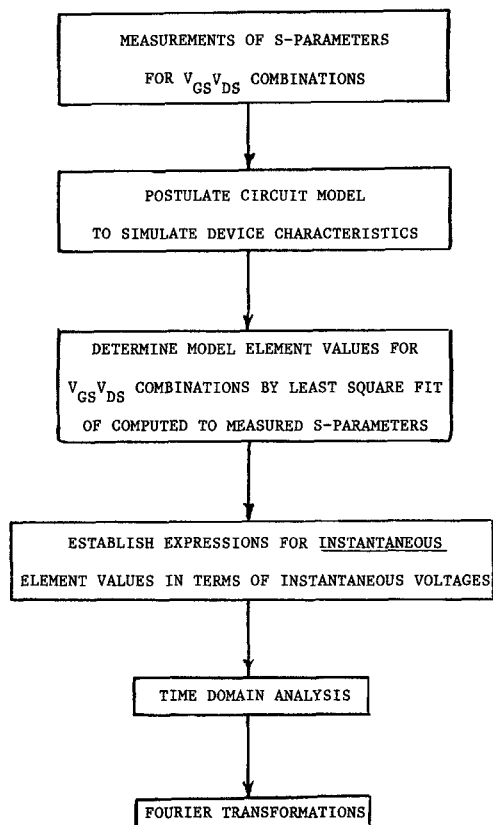
Fig. 5. Procedure for simulation of nonlinear GaAs MESFET performance.

Fig. 6. Fundamental output power versus incident power for a GaAs MESFET with a 50-Ω generator and output loads. Fundamental frequency is 2 GHz. Bias: $V_{GS} = -2.0$-V dc, $V_{DS} = 6.0$-V dc. Measured ——; Modeled – – – – –.

Fig. 7. Harmonic output power levels versus incident power for a GaAs MESFET with a 50-Ω generator and output loads. Fundamental frequency is 2 GHz. Bias: $V_{GS} = -2.0$-V dc, $V_{DS} = 6.0$-V dc. Measured ——; Modeled – – – – –. (a) Second harmonic. (b) Third harmonic. (c) Fourth harmonic. (d) Fifth harmonic.

mounted in a common-source configuration and biased at $V_{GS} = -2$-V dc and $V_{DS} = +6$-V dc. Simulations were performed for RF inputs at a fundamental frequency of 2 GHz and drive levels up to where 6 dB of gain compression occurs. The fundamental frequency of 2 GHz was selected to permit ease of laboratory measurements of the harmonic levels through the fifth (10 GHz). For each drive condition, Fourier analysis was employed to extract frequency-domain information from the waveforms. The sequence of steps leading to these large-signal simulations is summarized in Fig. 5. The comparison between experimental and model-predicted fundamental and harmonic output power levels are summarized in Figs. 6 and 7. The same excellent agreement was also observed in the case of third-order intermodulation distortion. The accurate predictions of high-order distortion products at frequencies up to 10 GHz have served to substantiate the usefulness of the model.

The above investigation deals with the resistive load-line case. This case permits simplification of the expression used to describe the nonlinear model element values as outlined in this paper. The generalized case, which does not rely on load-line assumption, allows simulation of device–circuit interaction for arbitrary loads. Currently, investigations are being conducted to establish the accuracy of such predictions.
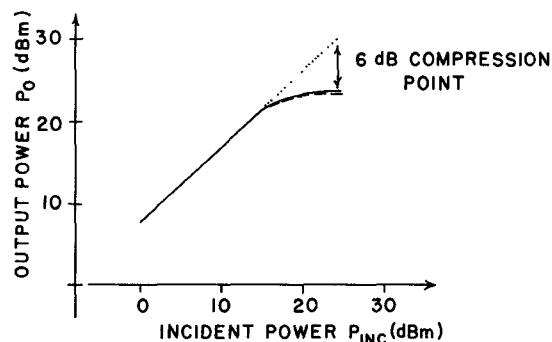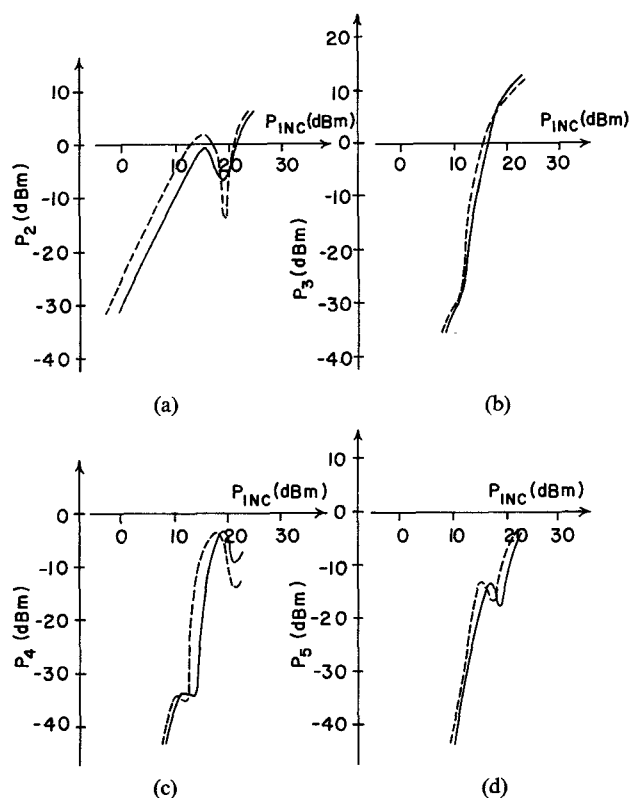
V. CONCLUSIONS

A technique for accurately predicting the nonlinear performance of GaAs FET's has been presented. It is based on the experimental characterization of the frequency and bias-dependent behavior of device small-signal S parameters. A nonlinear model is derived from this characterization. Fourier analysis of input and output waveforms simulated with this model yields predictions of fundamental, harmonic, and third-order intermodulation

power levels. Excellent agreement between laboratory measurements and model predictions has been demonstrated. The comparisons were made for signal levels up to where 6 dB of gain compression occurred.

ACKNOWLEDGMENT

The authors wish to thank Dr. B. E. Spielman, R. E. Neidert, and B. Sheleg for helpful comments and suggestions. We also thank H. Heddings for his assistance in the laboratory measurements.

REFERENCES

[1] H. A. Willing and P. de Santis, "Modeling of Gunn domain effects in GaAs MESFET's," Inst. Elec. Eng. Electron. Lett., vol. 13, no. 18, pp. 537–539, 1977.
[2] K. Lehovec and R. Zuleeg, "Voltage-current characteristics of GaAs J-FET's in the hot electron range," Inst. Elec. Eng. Solid-State Electron., vol. 13, pp. 1415–1429, 1970.
[3] R. W. H. Engelmann and C. A. Liechti, "Gunn domain formation in the saturated region of the GaAs MESFET's," in IEEE Int. Electron Devices Conf. Digest, 1976, pp. 351–354.
[4] R. S. Tucker and C. Rauscher, "Modeling the 3rd-order intermodulation-distortion properties of a GaAs FET," Electron. Lett., vol. 13, no. 17, pp. 508–510, 1977.

Surface-Oriented Transferred-Electron Devices

MICHAEL S. SHUR AND LESTER F. EASTMAN, FELLOW, IEEE

Abstract—The application of MESFET technology to the manufacturing of surface-oriented transferred-electron devices (TED's) with parameters close to GaAs MESFET's is discussed. The limitations related to the contact resistance, fringing capacitance, domain formation time, impact ionization, and heat sinking are analyzed for GaAs and InP devices. Our estimates show that the surface-oriented devices can be used as microwave LSA generators at higher frequencies than the conventional LSA diodes. In a domain mode, the surface-oriented TED's can yield low values of the power-delay product comparable to those of GaAs MESFET's at higher speeds. The analysis of impact ionization within a high-field domain leads to a conclusion that even InP logic devices with practical lengths of the active layer can be manufactured with doping densities up to $10^{17} cm^{-3}$. The estimate of the temperature rise indicates that a CW operation is possible for practical device parameters. Because the parameters of surface-oriented TED's are similar to those of GaAs MESFET's they may be manufactured using the rapidly developing GaAs integrated-circuit technology and used in combination with GaAs MESFET's.

I. INTRODUCTION

THE ADVANTAGES of GaAs MESFET's compared to Gunn devices may be partially related to a better technology and to a planar construction which provides better heat sinking. This technology now may be applied to manufacture surface-oriented Gunn devices (gateless FET's). Such devices have much in common with planar Gunn devices which have been extensively studied previously (see, for example, [1]-[6]) but their parameters, such as a very high doping density (up to $10^{17} cm^{-3}$), the small

thickness of the active layer (up to 0.15 μm), the large ratio of the active layer length over the thickness, etc., are close to the parameters of GaAs MESFET's. The surface-oriented MESFET's can be used as millimeter-wave generators and also as the components of monolithic GaAs integrated circuits where the combination of transferred-electron devices (TED's) and FET's proved to be especially effective [7].

In this paper we analyze the limitations of surface-oriented TED's related to the device physics and technology. We first derive the criteria of the LSA operation of the surface oriented TED's. It is followed by the estimate of a minimum switching time and a power-delay product in the domain mode and by the consideration of the limitations imposed by the impact ionization within the high-field domain. This calculation is relevant to the possible logic application of the devices. Finally, we consider a heat-sinking problem and derive a simple criterion which has to be fulfilled for a CW operation of the surface-oriented TED's.

II. FREQUENCY LIMITATIONS FOR SURFACE-ORIENTED GUNN GENERATORS

Our approach is similar to the one we used in [8] where we estimated the maximal frequency of generation for regular TED's. Our estimates are based on the simplest equivalent circuit shown in Fig. 1. Here R_c is a contact resistance, R_- is the equivalent negative resistance, and C is the equivalent capacitance. We calculated R_-/R_0 in [8]: